G.E.S's R. H. Sapat College of Engineering, Management Studies and Research, Nashik

Technical Bulletin

A.Y. 2023-24(Sem-II)

Department of

Electronics and Telecommunication Engineering

Department of Electronics and Telecommunication Engineering

Technical Bulletin

❖ Technical Activities

- **Enormous efforts are taken with an objective to embed sound academic fundamentals among students to formulate, analyze and solve real life problems related to their domain and area of expertise.**

- **An expert talk on "Opportunities of E & TC students in industry"**

Resource Person Dr. S. S. Sane
No. of Participants 75
Date 16 January 2024
Coordinator Dr. S. P. Agnihotri

- **An expert talk on "Industry 4.0 & Digitalization"**

Resource Person Mr. Narayan Banate (Siemens, Nashik)
No. of Participants 45
Date 27 January 2024
Coordinator Dr. S. P. Agnihotri

- **Skill development of girls students by "Mahindra Pride classroom for girl students"**

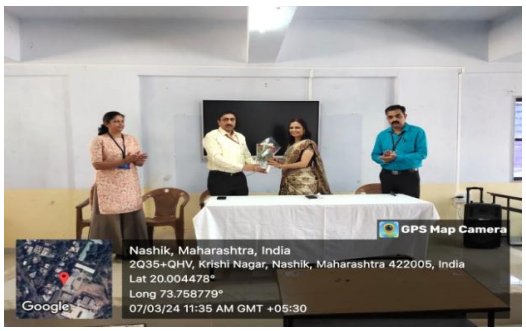
Resource Person **Ms. Ruby Padhi**
No. of Participants **35**
Date **18 January 2024 – 25 January 2024**
Coordinator **Mr. P. D. Lokhande**

- **An expert talk on "Opportunities of E & TC students in the field of aviation & drone technology"**

Resource Person **Mr. Vishal Joshi**
No. of Participants **70**
Date **27 February 2024**
Coordinator **Dr. S. P. Agnihotri**

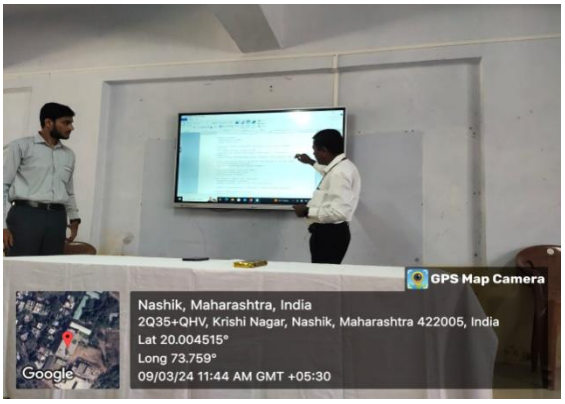
- **An expert talk on "Impact of Life Style on career"**

Resource Person **Dr. Prajakta Kulkarni**
No. of Participants **65**
Date **07 March 2024**
Coordinator **Mrs. G. R. Kawale**



- **An expert talk on “Network Simulator”**

Resource Person **Dr. S. R. Lahane**
No. of Participants **35**
Date **09 March 2024**
Coordinator **Dr. M. P. Joshi**



- **An expert talk on “Cyber Security & SAP”**

Resource Person **Ms. Semerpreet Kaur & team**
No. of Participants **52**
Date **11 March 2024**
Coordinator **Dr. M. P. Joshi**

- **An expert talk on “Start-ups & innovation”**

Resource Person **Eminent Speakers from industry**
No. of Participants **50**
Date **15 April 2024**
Coordinator **Dr. S. P. Agnihotri**

- **An expert talk on "Current challenges in Industry Global scenarios - Knowledge sharing"**

Resource Person Dr. A. R. Kulkarni
No. of Participants 45
Date 16 April 2024
Coordinator Dr. S. P. Agnihotri

- **Hands-on Workshop on "PCB Design & Fabrication"**

Resource Person Mr. D. M. Raut & Dr. K. V. Karad
No. of Participants 35
Date 03 – 04 April 2024
Coordinator Mr. D. M. Raut

- **Hands-on Workshop on "LATEX"**

Resource Person Dr. M. P. Joshi
No. of Participants 45
Date 02 April 2024
Coordinator Dr. M. P. Joshi

❖ Staff achievements

- Santosh Prabhakar Agnihotri and Mandar Padmakar Joshi, "Alternating current servo motor and programmable logic controller coupled with a pipe cutting machine based on human-machine interface using dandelion optimizer algorithm - attention pyramid convolution neural network," AIMS Electronics and Electrical Engineering, 8(1): pp. 1–27, 2024.

- Abhijit Kulkarni, Santosh Agnihotri, Arjun Kapile, Pratik Junagade, "Real Time Monitoring System Representing Offset Machine Press Counting and Report Generation," The Indian Journal of Technical Education, Vol. 47, No. 1, pp. 281 – 292, 2024.

- Prof. Dr. S. P. Agnihotri honored as "Best Teacher Award" by GES's R. H. Sapat College of Engineering, Management Studies and Research, Nashik.

- Mandar P. Joshi, Jayant G. Joshi, and Santosh P. Agnihotri, "Broadband and Compact Design Variations of Z-Shaped Printed Slot Microstrip Antenna," Progress In Electromagnetics Research C, Vol. 140, 75-84, 2024.

- J. G. Joshi, Mandar P. Joshi, S. Raghavan, S. S. Pattnaik, "Dual-Band Polyester-Based Wearable Bandpass Microstrip Filter Using Stepped Impedance Resonator.," International Journal of Microwave & Optical Technology Vol. 19, Issue 3, pp. 316 – 324, 2024.

- Mandar P. Joshi, Jayant G. Joshi, Shyam S. Pattnaik, "Dual Band Half-Hexagonal Slot Cut Wearable Microstrip Antenna," International Conference on Recent Technologies And Innovations In Electronics And Photonics: Towards Atmanirbhar Bharat, MIT WPU, Pune.

- Dr. M. P. Joshi honored as "Best Teacher Award" by GES's R. H. Sapat College of Engineering, Management Studies and Research, Nashik.

- Mrs. H. H. Kulkarni honored as "Best Teacher Award" by GES's R. H. Sapat College of Engineering, Management Studies and Research, Nashik.

- H. H. Kulkarni, "Ensemble Machine Learning Approaches with Bagging and Voting Classifier for Diabetes Disease prediction" International Conference on Business Intelligence and Data Analytics on 06-07 April 2024.

- Dr. K. V. Karad completed his PhD under G. H. Raisoni College of Engineering, Pune.

- K. V. Karad, V. S. Hendre, J. S. Rajput, M. P. Joshi, "Design and analysis of foam based flexible wearable MSA for healthcare applications," Book Title: Antennas for Industrial and Medical Applications with Optimization Techniques for Wireless Communication, CRC Press, 2024.

❖ Students achievements

- BE E & TC students Bhagwan Sonawane, Suchita Badgujar and Mayur More presented paper in A hybrid mode national conference IETE NTPC PRECCON -2024 at Pravara Rural Engineering College.

- BE E&TC student Bhavesh Patil awarded as the best batsman in resonance cricket tournament.

- TE student Niraj Chandratre represented Nashik District Zone at inter-zonal competition in Hockey during Year 2023-24 at Pune.

- Mr. Ishan Gholap from SE E & TC participated in Sanskrit Play at state level play competition.

- Mr. Ishan Gholap from SE E & TC participated in Marathi Play at state level play competition.

- Ms. Shrutika Mehendale awarded for her achievement in National Informatics Talent Search.

- Ms. Kshitija Khairnar & Ms. Tejswini Gaikwad from SE E & TC won gold medal in throw ball competition in Resonance 2k24.

- Ms. Kshitija Khairnar from SE E & TC participated in E-verse program at IIIT Hyderabad.

- Ms. Vaishnavi Gurav won best performance title in dance (Solo) in Resonance 2k24.

❖ **Upcoming Cutting Edge Technologies**

DRAMs: Technology and Beyond

(Dr. M. P. Joshi)

DDR5, the fifth-gen DRAM, demands digital-analogue finesse in its MC and DDR PHY. Unique timings, coupled with emerging tech like 3D XPoint, MRAM, and ReRAM, mark a paradigm shift. Memory is typically used for storing the data or program code needed by a computer processor to function. To accomplish this task, Dynamic random access memory (DRAM) is employed. DRAM is a common type of random access memory (RAM) used in personal computers (PCs), workstations, and servers. Random access allows the PC processor to access any part of the memory directly rather than proceeding sequentially from a starting place.

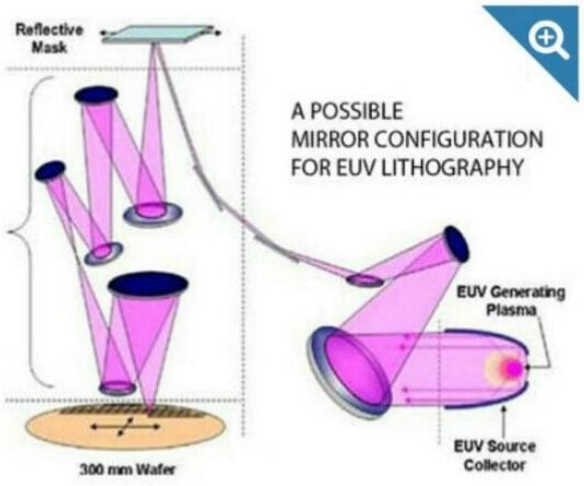


Fig. 1: EUV lithography for wafer fabrication (Credit: nist.gov)

How does DRAM work?

Memory is made of bits of data or program code arranged in a two-dimensional grid. DRAM stores bits of data in what's called a storage or memory cell, consisting of a capacitor and a transistor. The storage cells are typically organised in a rectangular configuration. When a charge is sent through a column, the transistor in the column is activated. A DRAM storage cell is dynamic, meaning that it needs to be refreshed or given a new electronic charge every few milliseconds to compensate for charge leaks from the capacitor. The memory cells work with other circuits that identify rows and columns, track the refresh process, instruct a cell whether or not to accept a charge, and read or restore data from a cell. DRAM is one option of semiconductor memory that a

system designer can use when building a computer. Typical sizes of DRAM are about 1 to 2GB in smartphones and tablets and 4 to 16GB in laptops.

Manufacturing processes involved in DRAM

DRAM manufacturing processes are referred to as 1x-nm, 1y-nm, 1z-nm, 1alpha-nm, and 1-beta. A particular dielectric layer is provided to achieve the capacitance for each bit cell. 1beta DRAMs are low-powered and have double data rate 5X (LPDDR5X), capable of delivering data at a rate of 8.5Gbps. Multi-pattern lithography, in combination with leading-edge process technology and advanced material capabilities, is required for the manufacture of 1beta node DRAMs. The introduction of enhanced dynamic voltage and frequency scaling extensions core (eDVFSC) techniques is used to improve power-saving controls of DRAMs.

1-gamma node DRAMs are coming

This advanced DRAM is expected to unlock exponential growth and opportunities for an increase in the digital economy. It is a major step to secure the semiconductor supply chain. Currently, Micron is a pioneer in DRAM manufacturing. Recently, it installed extreme ultraviolet (EUV) lithography production equipment at its A3 wafer fabrication unit in Taiwan.

In May 2023, Micron announced that it will be introducing this sophisticated pattern technology (EUV) to manufacture its next-generation DRAM, 1-gamma node. This technology is expected to provide the smallest cell size for DRAM. The downside of EUV lithography is that it needs multi-patterning, allowing 193nm lithography to considerably reduce the size of DRAM. Micron is combining new materials, tools, and novel techniques to improve its multi-patterned alignment.

Challenges Faced by DRAM Industry

One-die Error Correction Code (ECC) is a special feature in the DRAM industry that corrects bit errors in DRAM chips, increasing reliability and defect rates. ECC requires additional memory storage where ECC codes are stored at the time of memory write to DRAM. Hamming codes are used in such ECC schemes to provide single-bit and double-bit error detection per burst. Latest DRAMs like LPDDR5 and DDR5 support one-die ECC.

Row hammer

The same or adjacent rows are activated again and again, resulting in a loss or change of data contents in the rows that are not addressed. The latest versions of DRAM

LPDDR5/DDR5 support refresh management (including DRFM and ARFM) to compensate for this challenge

Device temperature

Users need to check with the DRAM vendor on the temperature range where DRAM should operate. Data integrity is lost at a level greater than a certain temperature.

Loss of power

DRAM may lose its contents due to a loss of power. So, a backup non-volatile memory is required where DRAM contents need to be copied before the power is lost. When power is regained, stored contents in non-volatile memory are written back to DRAM.

Next generation DRAMs

Current DRAMs increase latency and power consumption, known as the 'memory wall.' Next-generation DRAMs have come up with new features to overcome these challenges. Introduced by Intel in 2015, 3D XPoint is described as the next generation DRAM. 3D XPoint is based on a technology called Phase-Change Memory (PCM) and is used in SSDs and DIMMs. PCM stores information in the amorphous and crystalline phases.

Meanwhile, the industry is also developing other new memory types, such as Magnetoresistive RAM (MRAM) and Resistive RAM (ReRAM). Like 3D XPoint, MRAM and ReRAM can be made and sold as standalone devices.

3D XPoint is not sold as an embedded memory. In contrast, MRAM and ReRAM can also serve in the embedded memory markets. For MRAM, the industry is developing a next-generation technology called Spin-Transfer Torque MRAM (STT-MRAM). STT-MRAM uses the magnetism of electron spin to provide non-volatile properties in chips, combining the speed of SRAM and the non-volatility of flash with unlimited endurance.

In traditional memory, data is stored as an electric charge. In contrast, MRAM uses a magnetic tunnel junction (MTJ) memory cell for the storage element. Ferroelectric RAM (FRAM) is another technology to watch. Using a ferroelectric capacitor to store data, FRAM is a non-volatile memory with large storage capacity. Nantero, a private company, has more than 170 nanotube patents to replace DRAMs. It is possible to have hundreds and thousands of such nanotubes in every memory cell to form a network of resistive elements to form non-volatile random access memory (NVRAM). Undoubtedly, next-generation DRAMs are providing plenty of opportunities for OEMs.

❖ Out of Box

World's First Quad-Port SSD

The world's first quad-port SSD centralizes vehicle storage, offering connectivity and flexibility for advanced automotive applications with data center-level capabilities.

Micron Technology has announced that it is sampling the automotive-grade 4150AT SSD, which is the world's first quad-port SSD. This innovative drive can interface with up to four system-on-chips (SoCs) to centralize storage for software-defined intelligent vehicles. The 4150AT SSD incorporates features such as single-root input/output virtualization (SR-IOV), a PCIe Generation 4 interface, and a rugged automotive design, providing data centre-level flexibility and power for the automotive sector. The SSD achieves enterprise-class speeds in consumer vehicles, capable of handling over 600,000 input/output operations per second (IOPS) for random reads and over 100,000 IOPS for writes. This facilitates efficient data management from multiple SoCs simultaneously, making it an ideal solution for various vehicle systems like advanced driver-assistance systems (ADAS), in-vehicle infotainment (IVI), and AI-enabled cabin experiences.

Technical Bulletin Team

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